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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,938	10/15/2003	Yee-Chia Yeo	TSM03-0926	7692

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EXAMINER	
MOVVA, AMAR	

ART UNIT	PAPER NUMBER
2894	

MAIL DATE	DELIVERY MODE
07/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/685,938	YEO ET AL.	
	Examiner	Art Unit	
	AMAR MOVVA	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-14 and 17-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 6-14 17-19-+* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 6-7, 9-14, and 17-18 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto '894 in view of Paton '021.

a. Regarding claims 1-3,6-7, and 9-12:

i. Matsumoto discloses a semiconductor chip comprising: a semiconductor substrate (3,2,10c,10d, fig. 41) comprising an active region; a first structure (7a,9a, fig. 41) formed on the active region; and at least one dummy silicide structure (7c,9c, fig. 41) formed on the semiconductor substrate, wherein a first dummy silicide structure of the at least one dummy silicide structure is formed completely over an isolation region (4c, fig. 41), the isolation region comprising a dielectric material in a recess in the semiconductor substrate. The first structure is a transistor gate electrode of a transistor (fig. 41). A gate dielectric (4a, fig. 41) underlying the first structure, the gate dielectric comprising a high permittivity dielectric selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthanum

oxide, cerium oxide, titanium oxide, and tantalum oxide (lines 38-45, col. 22). The first structure and the at least one dummy silicide structure each comprises nickel silicide (lines 12-14, col. 24). The semiconductor substrate is a silicon substrate (lines 22-24, col. 21). The semiconductor substrate is a semiconductor-on-insulator substrate (fig. 41). A contact etch-stop layer (14, fig. 41) overlying portions of the first structure. A dielectric layer (11, fig. 41) overlying the first structure and the at least one dummy silicide structure. Matsumoto does not, however, expressly disclose that gate electrodes may be made of entirely nickel silicide.

ii. Paton discloses a semiconductor device wherein the gate electrode is made of entirely nickel silicide (fig. 6, ABSTRACT)

iii. It would have been obvious to one of ordinary skill in the art at the time of the invention to have made Matsumoto's gate electrodes (7,9, fig. 41) of entirely nickel silicide since it would reduce gate resistance thus improving device speed/performance [0010].

b. Regarding claims 13-14 and 17-18:

i. Matsumoto discloses an integrated circuit chip comprising: a substrate (3,2, fig. 41) having an active region and an isolation region (4c, fig. 41); a transistor (TR1, fig. 41) formed on the active region, the transistor having a source region, a drain region (6a1,6b1, fig. 41), and a silicided gate electrode (7a, 9a, fig. 41); and at least one dummy silicide structure (7c,9c,8 fig. 41) formed completely on the isolation region, the at

least one dummy silicide structure comprising a silicide layer (7c,9c, fig. 41) and a dielectric layer (8, fig. 41) being a separate layer from the isolation region. Electrical contacts are electrically coupled to the source region, the drain region, and the silicided gate- electrodes electrode (fig. 41). The silicided gate electrode and the at least one dummy silicide structure comprise nickel silicide (lines 12-14, col. 24). Matsumoto does not, however, expressly disclose that gate electrodes may be made of entirely nickel silicide.

ii. Paton discloses a semiconductor device wherein the gate electrode is made of entirely nickel silicide (fig. 6, ABSTRACT)

iii. It would have been obvious to one of ordinary skill in the art at the time of the invention to have made Matsumoto's gate electrodes (7,9, fig. 41) of entirely nickel silicide since it would reduce gate resistance thus improving device speed/performance [0010].

PLEASE NOTE: 3,2,10c,10d comprise the semiconductor substrate since the limitation only requires at least a portion of the substrate is semiconductor (e.g. a SOI substrate is commonly referred to as a semiconductor substrate in the art.

2. Claim1,8,13, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto '894 in view of Nakamura '574.

b. Regarding claims 8 and 13:

i. Matsumoto discloses a semiconductor chip comprising: a semiconductor substrate (3,2, fig. 41) comprising an active region; a first structure (7a, fig. 41) formed on the active region; and at least one dummy silicide structure (7c, fig. 41) formed on the semiconductor substrate, wherein a first dummy silicide structure of the at least one dummy silicide structure is formed completely over an isolation region (4c, fig. 41). However, Matsumoto does not expressly disclose gate electrodes made of entirely of NiGeSi.

ii. Nakamura discloses a semiconductor device wherein the gate electrode is made of entirely NiGeSi (col. 7).

iii. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used Nakamura's NiGeSi gat electrode in Matsumoto's device since since it would reduce gate resistance thus improving device speed/performance [0003] of Paton '021.

b. Regarding claims 13 and 19:

i. Matsumoto discloses an integrated circuit chip comprising: a substrate (3,2, fig. 41) having an active region and an isolation region (4c, fig. 41); a transistor (TR1, fig. 41) formed on the active region, the transistor having a source region, a drain region (6a1,6b1, fig. 41), and a silicided gate electrode (7a, fig. 41); and at least one dummy silicide structure (7c, fig. 2a) formed completely on the isolation region.

ii. However, Matsumoto does not expressly disclose gate electrodes made of entirely of NiGeSi.

iii. Nakamura discloses a semiconductor device wherein the gate electrode is made of entirely NiGeSi (col. 7).

iv. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used Nakamura's NiGeSi gat electrode in Matsumoto's device since since it would reduce gate resistance thus improving device speed/performance [0003] of Paton '021.

Response to Arguments

Applicant's arguments filed 7-14-08 have been fully considered but they are not persuasive.

a. Applicant argues that the term "isolation" regions has a meaning in the art to refer to structures used to isolate devices such as transistors and provides a reference, Wolf, to provide evidence to such effect. Wolf, however, merely discloses that regions such as STI and FOX are sufficient to be considered "isolation" regions not that they imply the necessary condition. Furthermore contrary to applicant's arguments Wieczorek '183 in [0049] provides for "gate isolation regions" (343,345 fig. 3f, 3g, 4) which are used as gate insulating films. Therefore one of ordinary skill in the art taking the broadest reasonable interpretation would have allowed for the interpretation of element 4c as an isolation region.

b. Applicant argues that elements 10c,10d cannot be part of the semiconductor substrate. Examiner notes that irrespective of the formation of the substrate, the only requirement that a "substrate" requires is that it support a layer thereupon. Furthermore examiner notes that limitations toward the formation of the device invoke the Product-by-Process doctrine. Product-by-process limitations are not limited by the manipulations of the recited steps, only the structure implied by the steps (MPEP 2113).

c. Applicant's remaining arguments with have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment on 1/11/2008 necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AMAR MOVVA whose telephone number is (571)272-9009. The examiner can normally be reached on 7:30 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Amar Movva
Examiner
Art Unit 2891

Am

/Bradley K Smith/
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